AMENDMENT OF THE CLAIMS

1. (Currently amended) A method of ~~shortening a single-bit error correction/double-bit error detection code for~~ detecting and correcting random bit errors in a digital transmission system using a shortened single-bit error correction/double-bit error detection code wherein data is scrambled after said error detection/correction code is applied over a set of data comprising:

obtaining unique syndromes for all combinations of multiplied errors completely confined to a set of data;

obtaining unique syndromes for those combinations of said multiplied errors occurring at the end of said set of data and overlapping a next set of data[[:]];

remembering the end unique syndrome types for allowing correction of said next set of data; and

obtaining syndromes for all combinations of said multiplied errors occurring at the beginning of said set of data that are at least unique per said end types.

2. (Original) The method according to claim 1 including the step of selecting a code requiring that shortening is kept minimal.

3. (Original) The method of either claim 1 or claim 2 wherein said error detection/correction code is such that syndromes characterizing bits in error at the beginning of a received descrambled set of data, when the number of said bits in error is less than the number of terms of the scrambling polynomial, need to be unique only per number of bits in error.

4. (Currently Amended) The method of claims 1 or 2 wherein said error detection/correction code is ~~a Hamming-like~~ an odd-weight extended Hamming code.

5. (Original) The method of claims 1 or 2 wherein each of said set of data comprises at least one 10Gb Ethernet 64B/66B block.

6, (Original) The method of claim 5 further comprising the step of inserting at least one control bit in said set of data, between each of said 10Gb Ethernet 64B/66B blocks, after said set of data has been scrambled.

7. (Currently amended) A method for transmitting data and associated redundant information allowing error detection and correction upon reception, said method comprising:

selecting a set of data:

computing forward error correction bits of said selected set of data according to a predetermined shortened forward error correction code;

merging said selected set of data and said forward error correction bits to form a packet;

scrambling said packet; and

transmitting said scrambled packet,

wherein said predetermined shortened forward error correction code is ~~determined~~ selected according to ~~syndrome~~ syndromes generated thereby.

8. (Currently Amended) A method for recovering information encoded in a received data packet, said received data packet being scrambled and containing shortened forward error correction bits, said method comprising:

descrambling said received data packet;

computing ~~the~~ a syndrome of said descrambled received data packet, wherein the syndrome is computed via the shortened forward error correction bits of the received data packet; and

if said syndrome is an all-zero syndrome, extracting the data from said received data packet.

9. (Original) The method of claim 8 including

else if said syndrome is not an all-zero syndrome,

determining the state of a status flag;

if said status flag is set to a first logical value, determining the number of bits in error in said received data packet according to said syndrome and,

if the number of bits in error in said received data packet is equal to the number of terms of the scrambling polynomial, extracting the data from said received data packet and correcting said extracted data.

10. (Original) The method of claim 9 further including:
else if the number of bits in error in said received data packet is less than the degree of the scrambling polynomial, setting said status flag to a second logical value for one packet cycle and setting a value, associated to said status flag, to the degree of the scrambling polynomial minus the number of bits in error in said received data packet, extracting the data from said received data packet and correcting said extracted data.

11. (Original) The method of claim 10 still further including:
else if said status flag is set to a second logical value, determining if the number of bits in error in said received flag and, if the number of bits in error in said received data packet is equal to said value associated to said flag, extracting the data from said received data packet and correcting said extracted data.

12. (Currently amended) The method set forth in claims 9 or 10 wherein correcting said extracted data ~~being~~ is done according to a predefined forward error correction code.

13. (New) An apparatus to correct an error in a data packet, the apparatus comprising:

a first circuit to generate a syndrome via forward error correction bits of the data packet, wherein the forward error correction bits are selected via a shortened group of vectors from an odd-weight group of vectors, wherein further the shortened group of vectors is based upon terms of a scrambler polynomial;

a second circuit to detect whether an end-of-packet error occurs in a previous data packet which precedes the data packet;

a third circuit to determine when multiplied errors of the error are confined to the data packet and when the multiplied errors affect a subsequent data packet which follows the data packet; and

a fourth circuit to correct the error when the generated syndrome differs from an all-zero syndrome, wherein the fourth circuit is arranged to:

correct the error of the data packet when no error occurs in the previous data packet and the multiplied errors are confined to the data packet;

correct the error of the data packet and set a flag which corresponds to a type of the error of the data packet when at least one of the multiplied errors affects the subsequent packet packet; and

correct the multiplied errors of the subsequent data packet based upon the set flag and the type of error of the first data packet.

14. (New) The apparatus of claim 13, further comprising a fifth circuit to receive the data packet.

15. (New) The apparatus of claim 13, further comprising a sixth circuit to decode the data packet when the packet is scrambled via the scrambler polynomial.

16. (New) The apparatus of claim 13, wherein the first circuit comprises an H-Matrix of the shortened group of vectors.

17. (New) The apparatus of claim 13, wherein the shortened group of vectors comprise odd-weight vectors α^0 through α^{914} from the group of odd-weight vectors α^0 through α^{1022}.

18. (New) The apparatus of claim 13, wherein the scrambler polynomial comprises $X^{58} + X^{19} + 1$.

19. (New) The apparatus of claim 13, wherein the shortened group of vectors corresponds code generating polynomial $G(x) = (X+1)(X^{10} + X^9 + X^7 + X^6 + X^4 + X^1 + 1)$.

20. (New) The apparatus of claim 13, wherein the type of the error of the data packet comprises a double bit end-of-packet error.